Dual, Low Power Video Op Amp

AD828

FEATURES

Excellent Video Performance
- Differential Gain & Phase Error of 0.01% & 0.05°

High Speed
- 130 MHz 3 dB Bandwidth (G = +2)
- 450 V/μs Slew Rate
- 80 ns Settling Time to 0.01%

Low Power
- 15 mA Max Power Supply Current

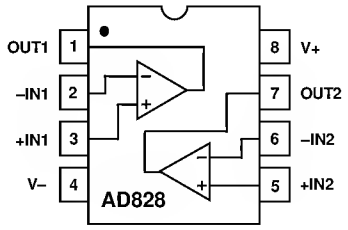
High Output Drive Capability:
- 50 mA Minimum Output Current per Amplifier
- Ideal for Driving Back Terminated Cables

Flexible Power Supply
- Specified for +5 V, ±5 V and ±15 V Operation
- ±3.2 V min Output Swing into a 150 Ω Load (V_S = ±5 V)

Excellent DC Performance
- 2.0 mV Input Offset Voltage

Available in 8-Pin SOIC and 8-Pin Plastic Mini-DIP

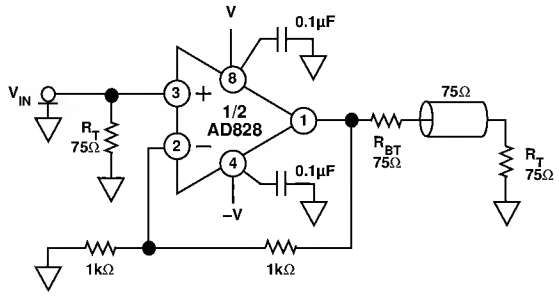
FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD828 is a low cost, dual video op amp optimized for use in video applications which require gains of +2 or greater and high output drive capability, such as cable driving. Due to its low power and single supply functionality, along with excellent differential gain and phase errors, the AD828 is ideal for power sensitive applications such as video cameras and professional video equipment.

With video specs like 0.1 dB flatness to 40 MHz and low differential gain and phase errors of 0.01% and 0.05°, along with 50 mA of output current per amplifier, the AD828 is an excellent choice for any video application. The 130 MHz gain bandwidth and 450 V/μs slew rate make the AD828 useful in many high speed applications including: video monitors, CATV, color copiers, image scanners and fax machines.

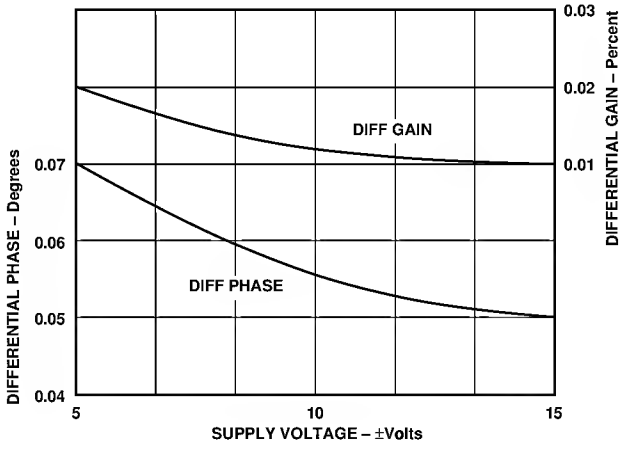


AD828 Video Line Driver

The AD828 is fully specified for operation with a single +5 V power supply and with dual supplies from ±5 V to ±15 V. This power supply flexibility, coupled with a very low supply current of 15 mA and excellent ac characteristics under all power supply conditions, make the AD828 the ideal choice for many demanding yet power sensitive applications.

The AD828 is a voltage feedback op amp which excels as a gain stage (gains >+2) or active filter in high speed and video systems and achieves a settling time of 45 ns to 0.1%, with a low input offset voltage of 2 mV max.

The AD828 is available in low cost, small 8-pin plastic mini-DIP and SOIC packages.



REV. A

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Tel: 617/329-4700 **Fax: 617/326-8703**

AD828– SPECIFICATIONS (@ T_A = +25°C, unless otherwise noted)

Parameter	Conditions	V_S	AD828 Min	AD828 Typ	AD828 Max	Units
DYNAMIC PERFORMANCE						
–3 dB Bandwidth	Gain = +2	±5 V	60	85		MHz
		±15 V	100	130		MHz
		0, +5 V	30	45		MHz
	Gain = –1	±5 V	35	55		MHz
		±15 V	60	90		MHz
		0, +5 V	20	35		MHz
Bandwidth for 0.1 dB Flatness	Gain = +2	±5 V	30	43		MHz
	C_C = 1 pF	±15 V	30	40		MHz
		0, +5 V	10	18		MHz
	Gain = –1	±5 V	15	25		MHz
	C_C = 1 pF	±15 V	30	50		MHz
		0, +5 V	10	19		MHz
Full Power Bandwidth[1]	V_{OUT} = 5 V p-p					
	R_{LOAD} = 500 Ω	±5 V		22.3		MHz
	V_{OUT} = 20 V p-p					
	R_{LOAD} = 1 kΩ	±15 V		7.2		MHz
Slew Rate	R_{LOAD} 1 kΩ	±5 V	300	350		V/µs
	Gain = –1	±15 V	400	450		V/µs
		0, +5 V	200	250		V/µs
Settling Time to 0.1%	–2.5 V to +2.5 V	±5 V		45		ns
	0 V–10 V Step, A_V = –1	±15 V		45		ns
to 0.01%	–2.5 V to +2.5 V	±5 V		80		ns
	0 V–10 V Step, A_V = –1	±15 V		80		ns
NOISE/HARMONIC PERFORMANCE						
Total Harmonic Distortion	F_C = 1 MHz	±15 V		–78		dB
Input Voltage Noise	f = 10 kHz	±5 V, ±15 V		10		nV/$\sqrt{\text{Hz}}$
Input Current Noise	f = 10 kHz	±5 V, ±15 V		1.5		pA/$\sqrt{\text{Hz}}$
Differential Gain Error	NTSC	±15 V		0.01	0.02	%
(R_L = 150 Ω)	Gain = +2	±5 V		0.02	0.03	%
		0, +5 V		0.08		%
Differential Phase Error	NTSC	±15 V		0.05	0.09	Degrees
(R_L = 150 Ω)	Gain = +2	±5 V		0.07	0.1	Degrees
		0, +5 V		0.1		Degrees
DC PERFORMANCE						
Input Offset Voltage		±5 V, ±15 V		0.5	2	mV
	T_{MIN} to T_{MAX}				3	mV
Offset Drift				10		µV/°C
Input Bias Current		±5 V, ±15 V		3.3	6.6	µA
	T_{MIN}				10	µA
	T_{MAX}				4.4	µA
Input Offset Current		±5 V, ±15 V		25	200	nA
	T_{MIN} to T_{MAX}				500	nA
Offset Current Drift				0.3		nA/°C
Open Loop Gain	V_{OUT} = ±2.5 V	±5 V				
	R_{LOAD} = 500 Ω		3	5		V/mV
	T_{MIN} to T_{MAX}		2			V/mV
	R_{LOAD} = 150 Ω		2	4		V/mV
	V_{OUT} = ±10 V	±15 V				
	R_{LOAD} = 1 kΩ		5.5	9		V/mV
	T_{MIN} to T_{MAX}		2.5			V/mV
	V_{OUT} = ±7.5 V	±15 V				
	R_{LOAD} = 150 Ω (50 mA Output)		3	5		V/mV
INPUT CHARACTERISTICS						
Input Resistance				300		kΩ
Input Capacitance				1.5		pF
Input Common-Mode Voltage Range		±5 V	+3.8	+4.3		V
			–2.7	–3.4		V
		±15 V	+13	+14.3		V
			–12	–13.4		V
		0, +5 V	+3.8	+4.3		V
			+1.2	+0.9		V
Common-Mode Rejection Ratio	V_{CM} = +2.5 V, T_{MIN} to T_{MAX}	±5 V	82	100		dB
	V_{CM} = ±12 V	±15 V	86	120		dB
	T_{MIN} to T_{MAX}	±15 V	84	100		dB

Parameter	Conditions	V_S	Min	Typ	Max	Units
OUTPUT CHARACTERISTICS						
Output Voltage Swing	R_{LOAD} = 500 Ω	±5 V	3.3	3.8		±V
	R_{LOAD} = 150 Ω	±5 V	3.2	3.6		±V
	R_{LOAD} = 1 kΩ	±15 V	13.3	13.7		±V
	R_{LOAD} = 500 Ω	±15 V	12.8	13.4		±V
			+1.5,			
	R_{LOAD} = 500 Ω	0, +5 V	+3.5			±V
Output Current		±15 V	50			mA
		±5 V	40			mA
		0, +5 V	30			mA
Short-Circuit Current		±15 V		90		mA
Output Resistance	Open Loop			8		Ω
MATCHING CHARACTERISTICS						
Dynamic						
Crosstalk	f = 5 MHz	±15 V		–80		dB
Gain Flatness Match	G = +1, f = 40 MHz	±15 V		0.2		dB
Skew Rate Match	G = –1	±15 V		10		V/µs
DC						
Input Offset Voltage Match	T_{MIN} to T_{MAX}	±5 V, ±15 V		0.5	2	mV
Input Bias Current Match	T_{MIN} to T_{MAX}	±5 V, ±15 V		0.06	0.8	µA
Open-Loop Gain Match	V_O = ±10 V, R_L = 1 kΩ, T_{MIN} to T_{MAX}	±15 V		0.01	0.15	mV/V
Common-Mode Rejection Ratio Match	V_{CM} = ±12 V, T_{MIN} to T_{MAX}	±15 V	80	100		dB
Power Supply Rejection Ratio Match	±5 V to ±15 V, T_{MIN} to T_{MAX}		80	100		dB
POWER SUPPLY						
Operating Range	Dual Supply		±2.5		±18	V
	Single Supply		+5		+36	V
Quiescent Current		±5 V		14.0	15	mA
	T_{MIN} to T_{MAX}	±5 V		14.0	15	mA
	T_{MIN} to T_{MAX}	±5 V			15	mA
Power Supply Rejection Ratio	V_S = ±5 V to ±15 V, T_{MIN} to T_{MAX}		80	90		dB

NOTES
[1]Full power bandwidth = slew rate/2 π V_{PEAK}.
Specifications subject to change without notice.

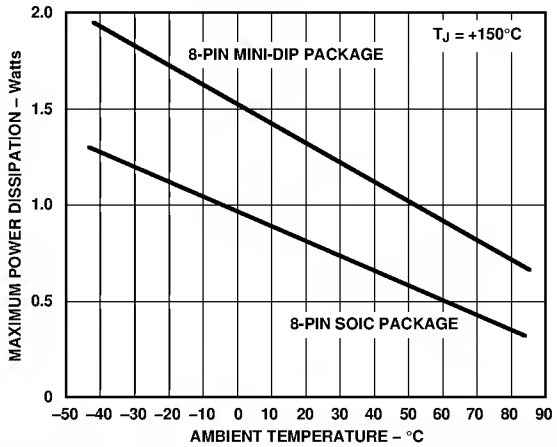
ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage ..... ±18 V
Internal Power Dissipation[2]
Plastic DIP (N) ..... See Derating Curves
Small Outline (R) ..... See Derating Curves
Input Voltage (Common Mode) ..... ±V_S
Differential Input Voltage ..... ±6 V
Output Short Circuit Duration ..... See Derating Curves
Storage Temperature Range (N, R) ..... –65°C to +125°C
Operating Temperature Range ..... –40°C to +85°C
Lead Temperature Range (Soldering 10 sec) ..... +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Specification is for device in free air:
8-Pin Plastic DIP Package: θ_{JA} = 100°C/Watt
8-Pin SOIC Package: θ_{JA} = 155°C/Watt

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD828AN	–40°C to +85°C	8-Pin Plastic DIP	N-8
AD828AR	–40°C to +85°C	8-Pin Plastic SOIC	R-8
AD828AR-REEL	–40°C to +85°C	8-Pin Plastic SOIC	R-8



Maximum Power Dissipation vs. Temperature for Different Package Types

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD828 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

AD828- Typical Characteristics

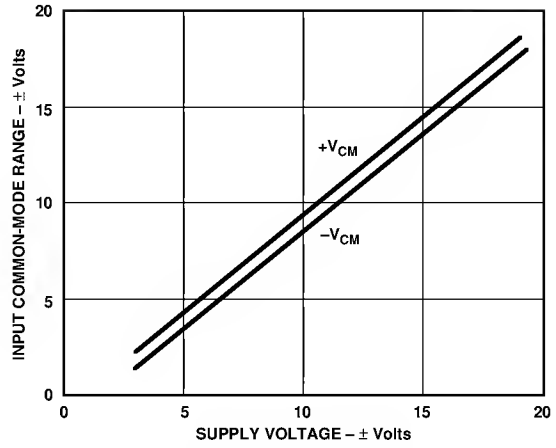


Figure 1. Common-Mode Voltage Range vs. Supply Voltage

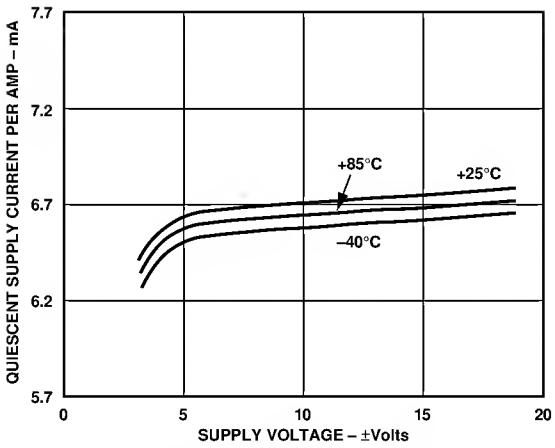


Figure 4. Quiescent Supply Current per Amp vs. Supply Voltage for Various Temperatures

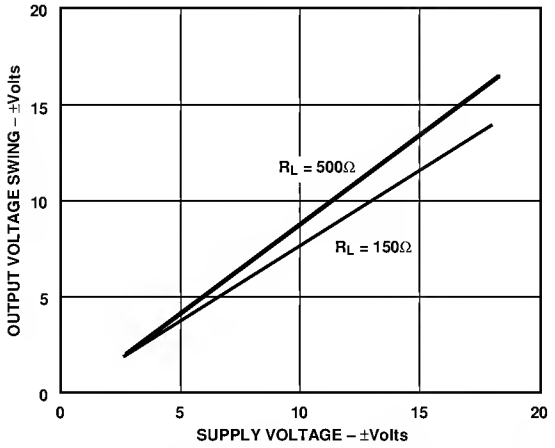


Figure 2. Output Voltage Swing vs. Supply Voltage

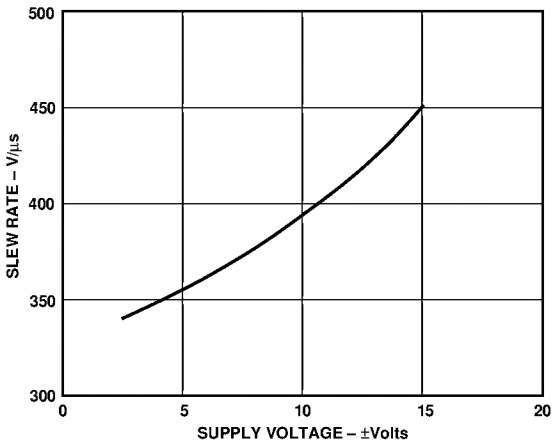


Figure 5. Slew Rate vs. Supply Voltage

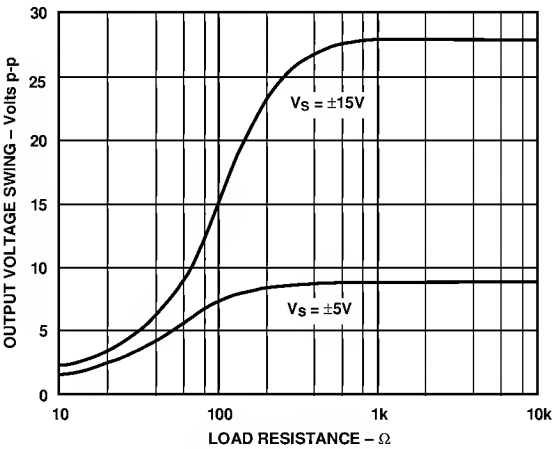


Figure 3. Output Voltage Swing vs. Load Resistance

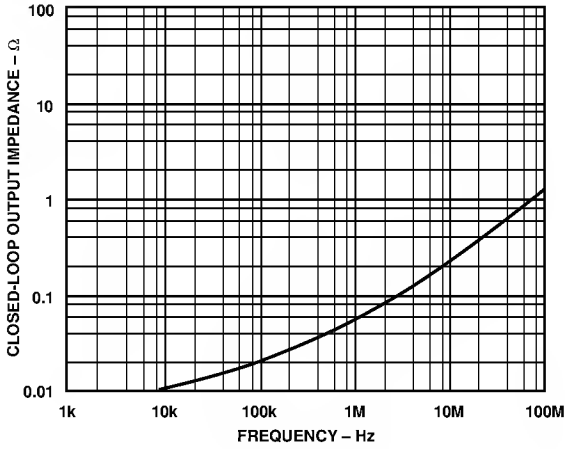


Figure 6. Closed-Loop Output Impedance vs. Frequency

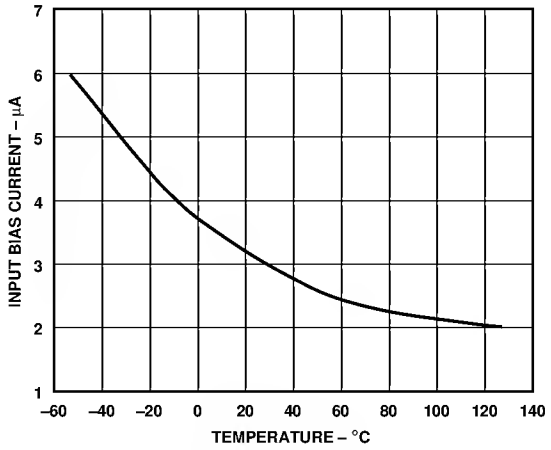


Figure 7. Input Bias Current vs. Temperature

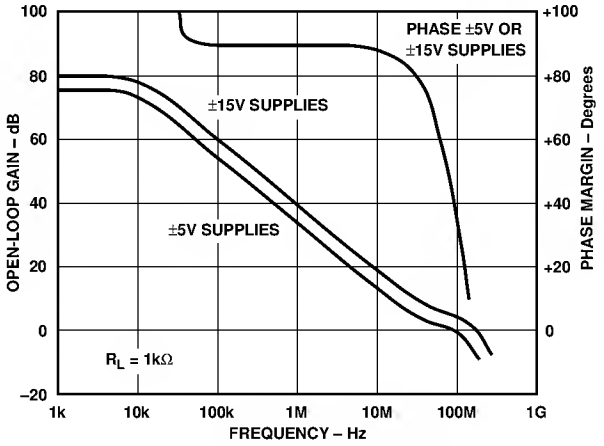


Figure 10. Open-Loop Gain and Phase Margin vs. Frequency

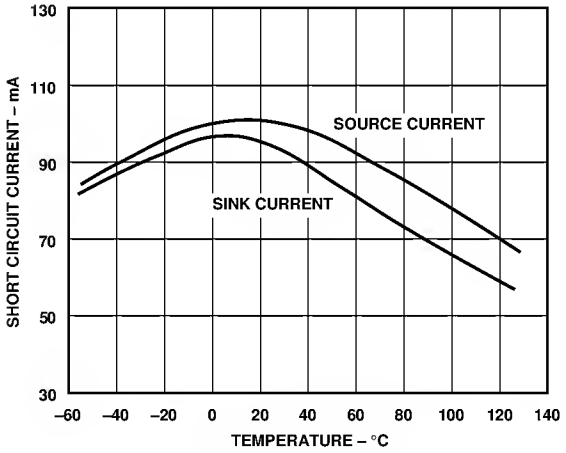


Figure 8. Short Circuit Current vs. Temperature

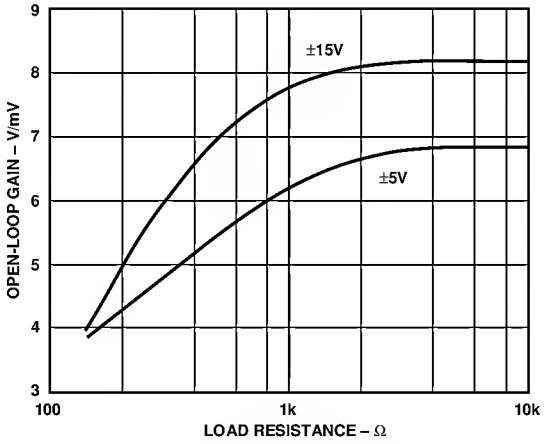


Figure 11. Open-Loop Gain vs. Load Resistance

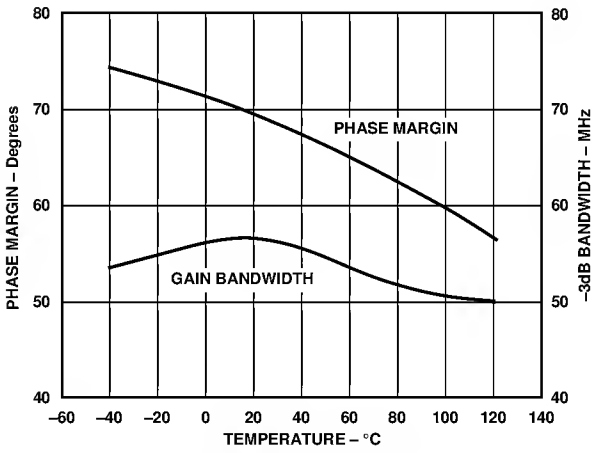


Figure 9. -3 dB Bandwidth and Phase Margin vs. Temperature, Gain=+2

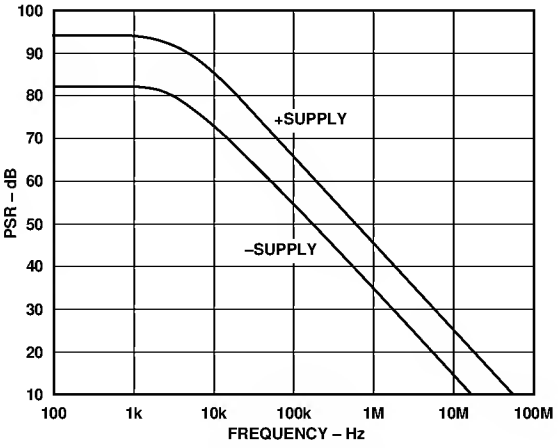


Figure 12. Power Supply Rejection vs. Frequency

AD828- Typical Characteristics

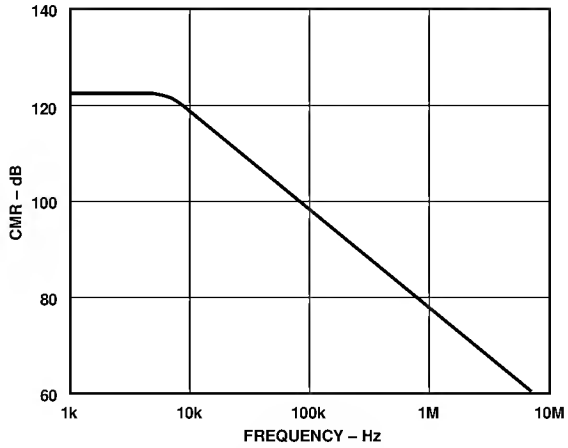


Figure 13. Common-Mode Rejection vs. Frequency

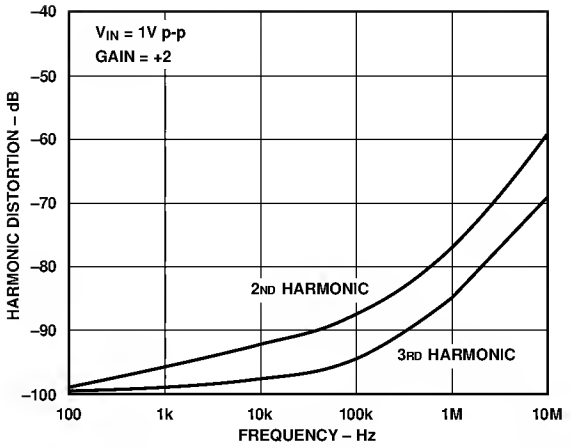


Figure 16. Harmonic Distortion vs. Frequency

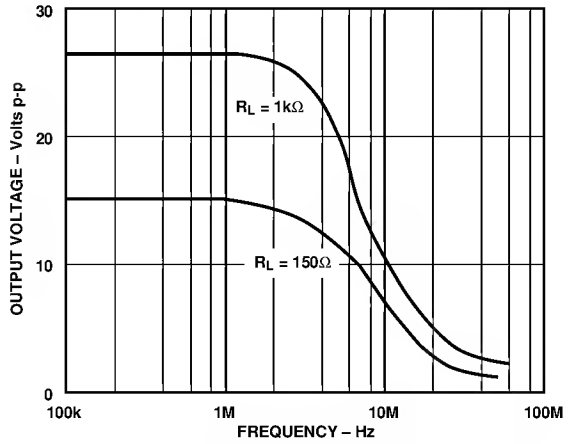


Figure 14. Large Signal Frequency Response

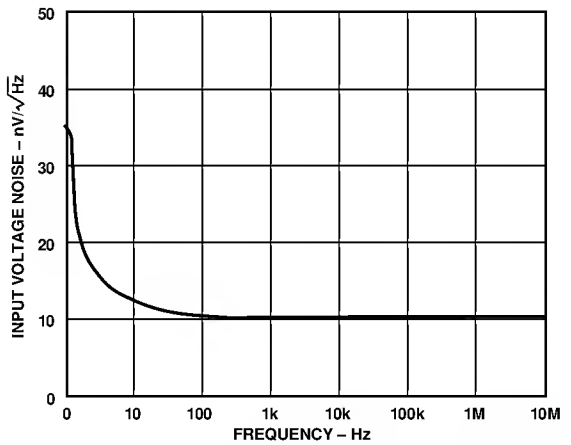


Figure 17. Input Voltage Noise Spectral Density vs. Frequency

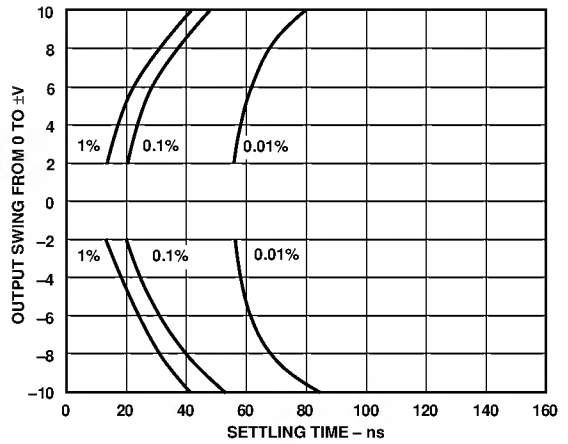


Figure 15. Output Swing and Error vs. Settling Time

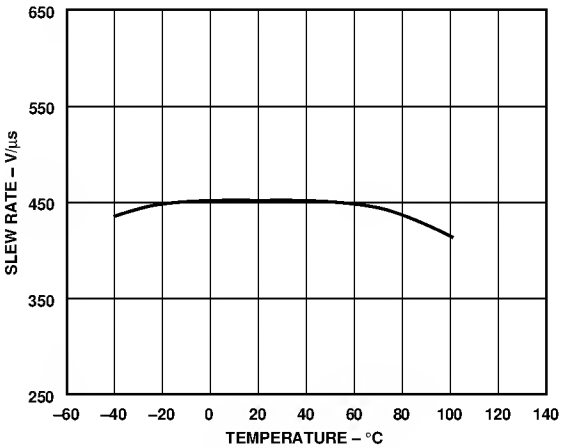


Figure 18. Slew Rate vs. Temperature

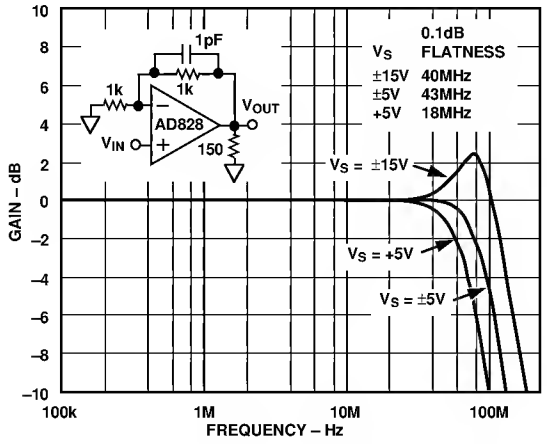


Figure 19. Closed-Loop Gain vs. Frequency

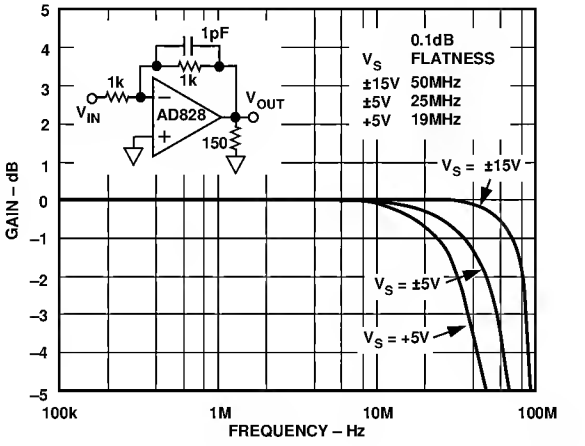


Figure 22. Closed-Loop Gain vs. Frequency, G =–1

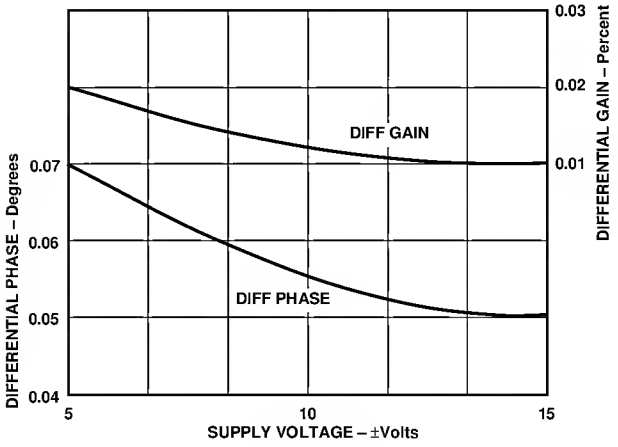


Figure 20. Differential Gain and Phase vs. Supply Voltage

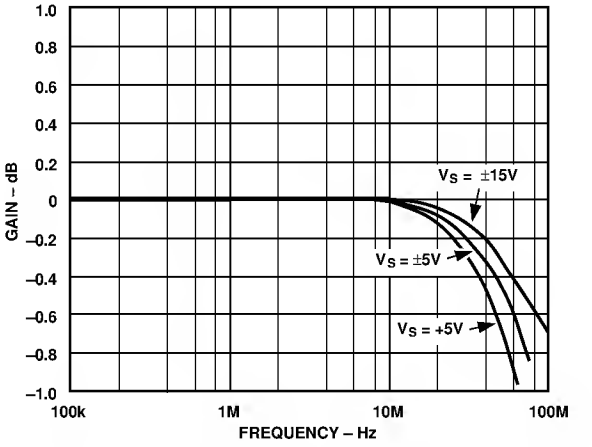


Figure 23. Gain Flatness Matching vs. Supply, G =+2

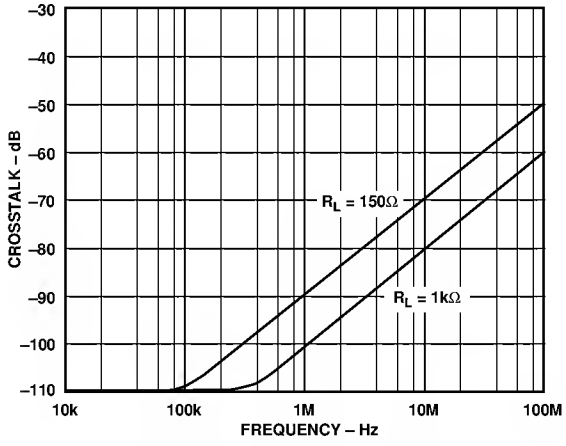


Figure 21. Crosstalk vs. Frequency

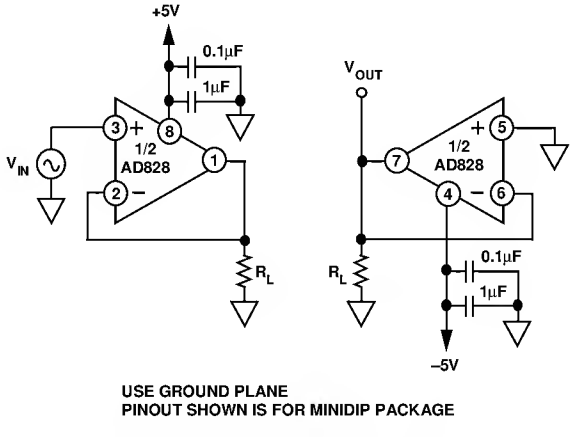


Figure 24. Crosstalk Test Circuit

AD828- Typical Characteristics

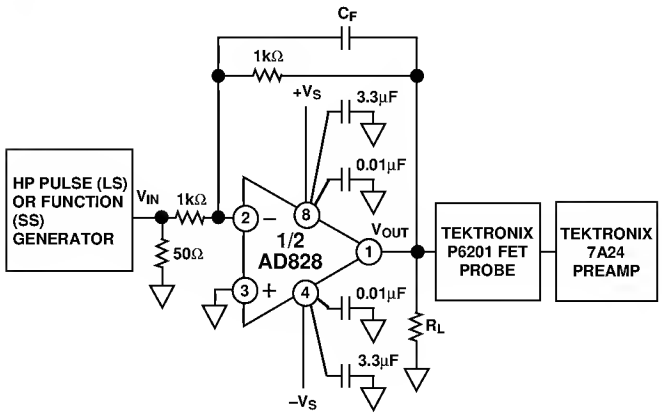


Figure 25. Inverting Amplifier Connection

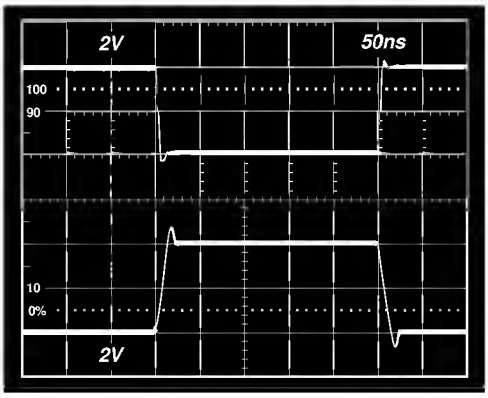


Figure 26. Inverter Large Signal Pulse Response ±5 V_S, C_F = 1 pF, R_L = 1 kΩ

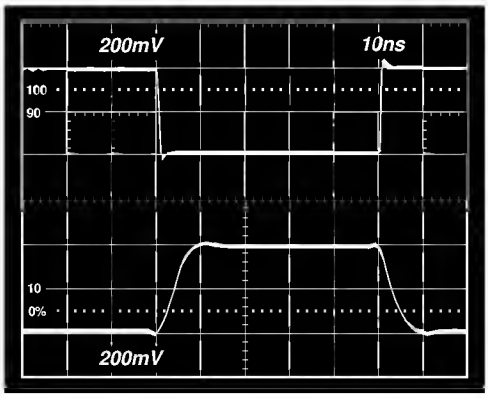


Figure 27. Inverter Small Signal Pulse Response ±5 V_S, C_F = 1 pF, R_L = 150 Ω

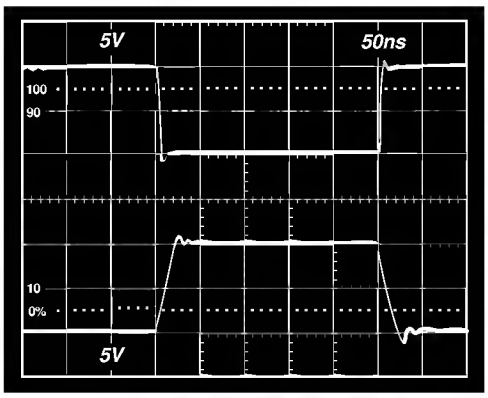


Figure 28. Inverter Large Signal Pulse Response ±15 V_S, C_F = 1 pF, R_L = 1 kΩ

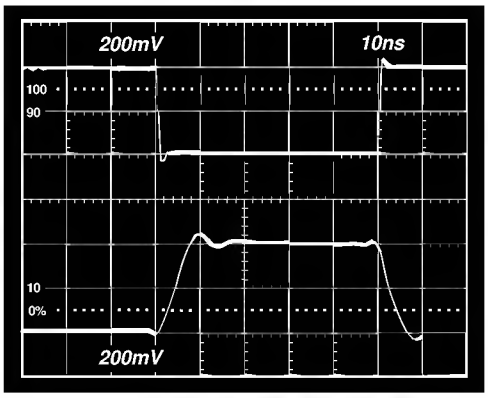


Figure 29. Inverter Small Signal Pulse Response ±15 V_S, C_F = 1 pF, R_L = 150 Ω

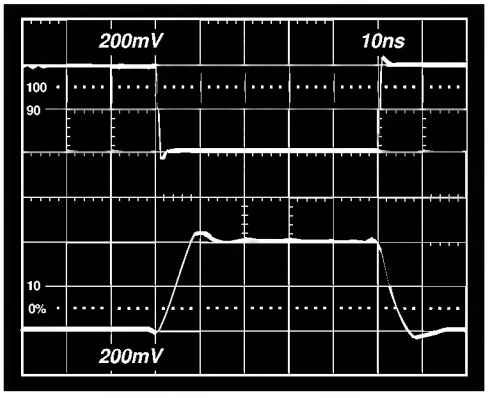


Figure 30. Inverter Small Signal Pulse Response ±5 V_S, C_F = 0 pF, R_L = 150 Ω

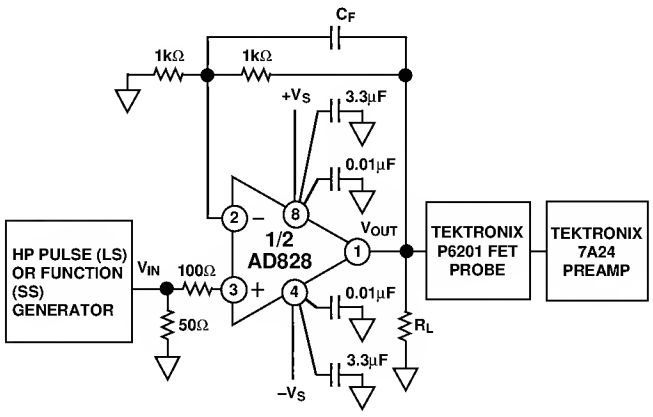


Figure 31. Noninverting Amplifier Connection

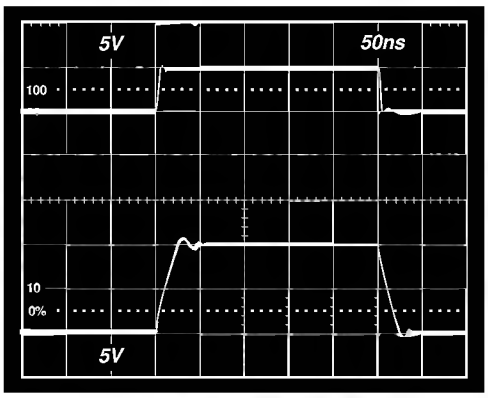


Figure 34. Noninverting Large Signal Pulse Response ±15 V_S, C_F =1 pF, R_L =1 kΩ

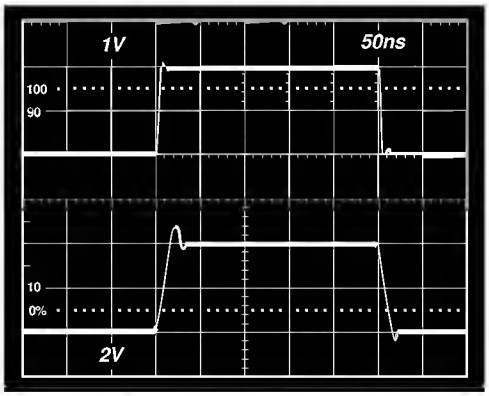


Figure 32. Noninverting Large Signal Pulse Response ±5 V_S, C_F =1 pF, R_L =1 kΩ

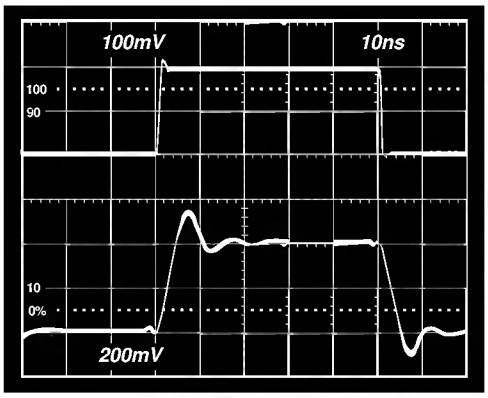


Figure 35. Noninverting Small Signal Pulse Response ±15 V_S, C_F =1 pF, R_L =150 Ω

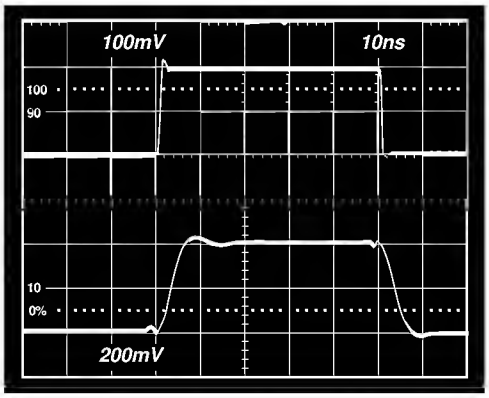


Figure 33. Noninverting Small Signal Pulse Response ±5 V_S, C_F =1 pF, R_L =150 Ω

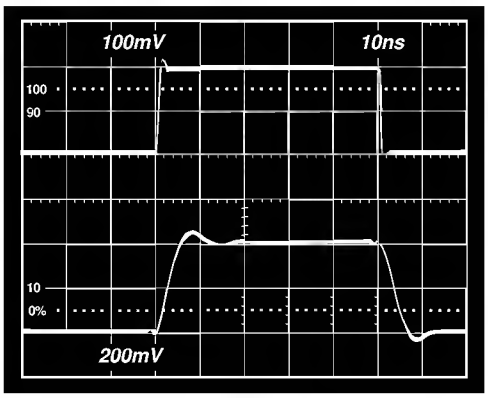


Figure 36. Noninverting Small Signal Pulse Response ±5 V_S, C_F =0 pF, R_L =150 Ω

THEORY OF OPERATION

The AD828 is a low cost, dual video operational amplifier designed to excel in high performance, high output current video applications.

The AD828 (Figure 37) consists of a degenerated NPN differential pair driving matched PNPs in a folded-cascode gain stage. The output buffer stage employs emitter followers in a class AB amplifier that delivers the necessary current to the load while maintaining low levels of distortion.

The AD828 will drive terminated cables and capacitive loads of 10 pF or less. As the closed-loop gain is increased, the AD828 will drive heavier cap loads without oscillating.

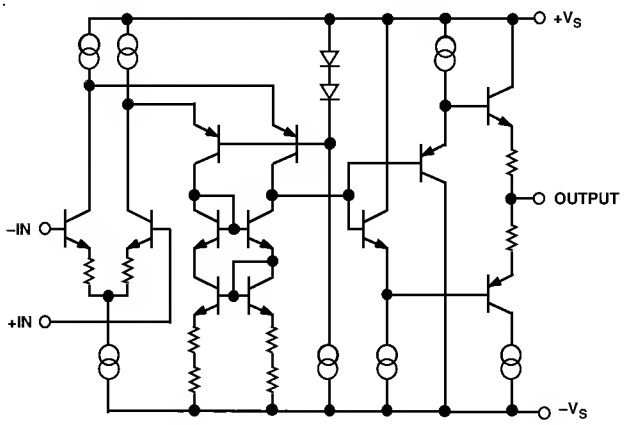


Figure 37. AD828 Simplified Schematic

INPUT CONSIDERATIONS

An input protection resistor (R_{IN} in Figure 31) is required in circuits where the input to the AD828 will be subjected to transient or continuous overload voltages exceeding the ±6 V maximum differential limit. This resistor provides protection for the input transistors by limiting their maximum base current.

For high performance circuits, it is recommended that a "balancing" resistor be used to reduce the offset errors caused by bias current flowing through the input and feedback resistors. The balancing resistor equals the parallel combination of R_{IN} and R_F and thus provides a matched impedance at each input terminal. The offset voltage error will then be reduced by more than an order of magnitude.

APPLYING THE AD828

The AD828 is a breakthrough dual amp that delivers precision and speed at low cost with low power consumption. The AD828 offers excellent static and dynamic matching characteristics, combined with the ability to drive heavy resistive loads.

As with all high frequency circuits, care should be taken to maintain overall device performance as well as their matching. The following items are presented as general design considerations.

Circuit Board Layout

Input and output runs should be laid out so as to physically isolate them from remaining runs. In addition, the feedback resistor of each amplifier should be placed away from the feedback resistor of the other amplifier, since this greatly reduces interamp coupling.

Choosing Feedback and Gain Resistors

In order to prevent the stray capacitance present at each amplifier's summing junction from limiting its performance, the feedback resistors should be ≤ 1 kΩ. Since the summing junction capacitance may cause peaking, a small capacitor (1 pF–5 pF) may be paralleled with Rf to neutralize this effect. Finally, sockets should be avoided, because of their tendency to increase interlead capacitance.

Power Supply Bypassing

Proper power supply decoupling is critical to preserve the integrity of high frequency signals. In carefully laid out designs, decoupling capacitors should be placed in close proximity to the supply pins, while their lead lengths should be kept to a minimum. These measures greatly reduce undesired inductive effects on the amplifier's response.

Though two 0.1 µF capacitors will typically be effective in decoupling the supplies, several capacitors of different values can be paralleled to cover a wider frequency range.

PARALLEL AMPS PROVIDE 100 mA TO LOAD

By taking advantage of the superior matching characteristics of the AD828, enhanced performance can easily be achieved by employing the circuit in Figure 38. Here, two identical cells are paralleled to obtain even higher load driving capability than that of a single amplifier (100 mA min guaranteed). R1 and R2 are included to limit current flow between amplifier outputs that would arise in the presence of any residual mismatch.

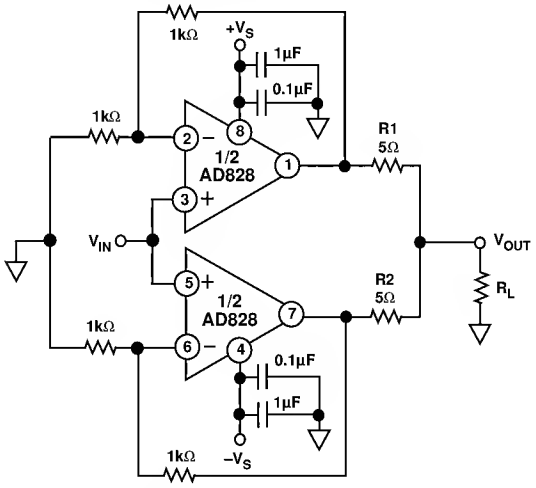


Figure 38. Parallel Amp Configuration

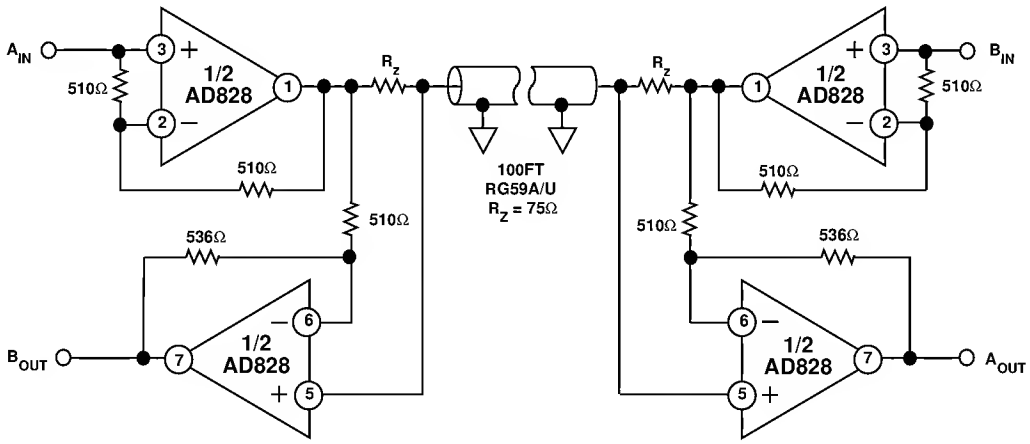


Figure 39. Bidirectional Transmission CKT

Full-Duplex Transmission

Superior load handling capability (50 mA min/amp), high bandwidth, wide supply voltage range and excellent crosstalk rejection makes the AD828 an ideal choice even for the most demanding high speed transmission applications.

The schematic below shows a pair of AD828s configured to drive 100 feet of coaxial cable in a full-duplex fashion.

Two different NTSC video signals are simultaneously applied at A_{IN} and B_{IN} and are recovered at A_{OUT} and B_{OUT}, respectively. This situation is illustrated in Figures 40 and 41. These pictures clearly show that each input signal appears undisturbed at its output, while the unwanted signal is eliminated at either receiver.

The transmitters operate as followers, while the receivers' gain is chosen to take full advantage of the AD828's unparalled CMRR. (In practice this gain is adjusted slightly from its theoretical value to compensate for cable nonidealities and losses.) R_Z is chosen to match the characteristic impedance of the cable employed.

Finally, although a coaxial cable was used, the same topology applies unmodified to a variety of cables (such, as twisted pairs often used in telephony).

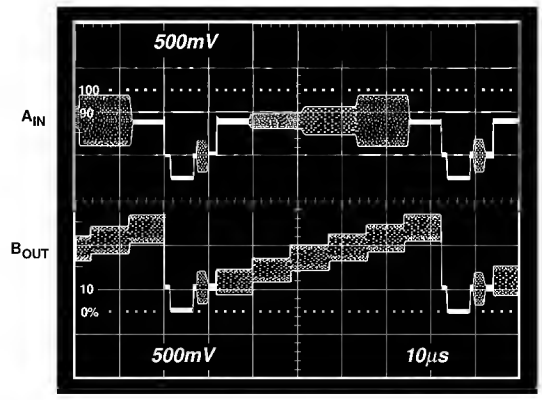


Figure 40. A Transmission/B Reception

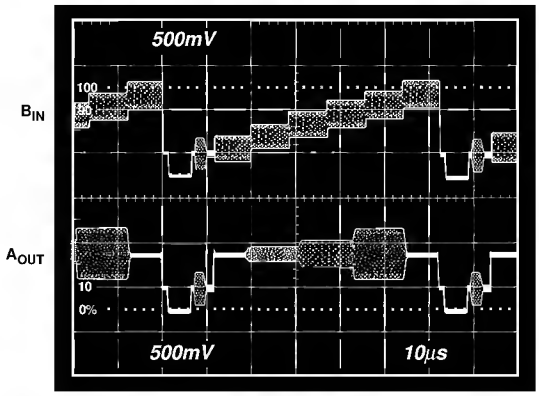


Figure 41. B Transmission/A Reception

A High Performance Video Line Driver

The buffer circuit shown in Figure 42 will drive a back-terminated 75 Ω video line to standard video levels (1 V p-p) with 0.1 dB gain flatness to 40 MHz with only 0.05° and 0.01% differential phase and gain at the 3.58 MHz NTSC subcarrier frequency. This level of performance, which meets the requirements for high-definition video displays and test equipment, is achieved using only 7 mA quiescent current/amplifier.

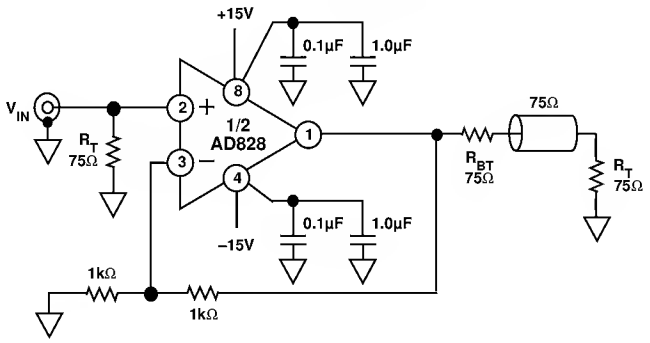


Figure 42. Video Line Driver

LOW DISTORTION LINE DRIVER

The AD828 can quickly be turned into a powerful, low distortion line driver (see Figure 43). In this arrangement the AD828 can comfortably drive a 75 Ω back-terminated cable, with a 5 MHz, 2 V p-p input; all of this while achieving the harmonic distortion performance outlined in the following table.

Configuration	2nd Harmonic
1. No Load	–78.5 dBm
2. 150 Ω R_L Only	–63.8 dBm
3. 150 Ω R_L 7.5 Ω R_C	–70.4 dBm

In this application one half of the AD828 operates at a gain of 2.1 and supplies the current to the load, while the other provides the overall system gain of 2. This is important for two reasons: the first is to keep the bandwidth of both amplifiers the same, and the second is to preserve the AD828's ability to operate from low supply voltage. R_C varies with the load and must be chosen to satisfy the following equation:

$$R_C = M R_L,$$

where M is defined by $[(M + 1) G_S = G_D]$ and G_D = Driver's Gain, G_S = System Gain.

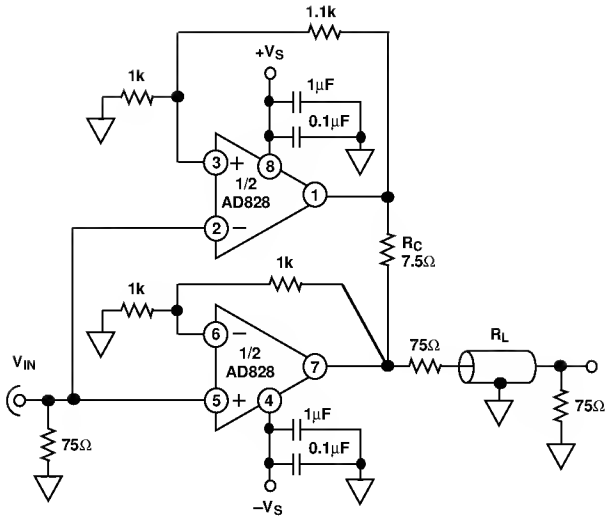


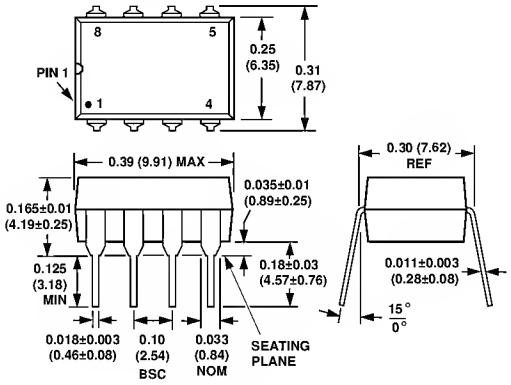
Figure 43. Low Distortion Amplifier

C1823a–7.5–8/94

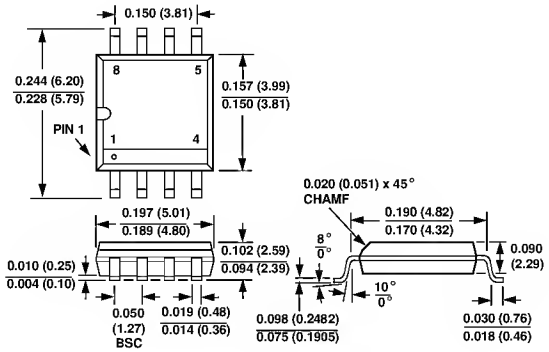
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Pin Plastic Mini-DIP (N) Package



8-Pin SO (R) Package



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